In the Claims:

1. (Currently Amended) An apparatus comprising:

an input stage with

an NMOS transistor doublet having a first differential input for receiving input signals,

a PMOS transistor doublet having a second differential input for receiving input signals, and

a plurality of switches configured to ~~receiving and selectively~~ couple ~~directing~~ analog input signals to the ~~only to one of either said~~ first differential input ~~or said second differential input responsive to a switching signal and for connecting~~ and couple the ~~other one of the first and~~ second differential input[[s]] to a first reference voltage in response to a ~~responsive to the~~ switching signal being a first value, and configured to couple the analog input signals to the second differential input and couple the first differential input to a second reference voltage in response to the switching signal being a second value, wherein the coupling of analog inputs signals and the first and second reference voltages causes ~~whereby the input stage is configured to keep~~ the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet to remain constant over the entire input range.

2. (Previously presented) The apparatus of claim 1, wherein the plurality of switches direct the analog input signals to said first differential input if the input signals have positive gamma data and to said second differential input if the input signals have negative gamma data.

3. (Previously presented) The apparatus of claim 1, wherein the NMOS transistor doublet comprises two NMOS transistors, each having a gate, whereby the gate of the first of the two NMOS transistors is connectable to a first input node via a first switch of the plurality of switches and the gate of the second of the two NMOS transistors is connectable to a second input node via a second switch of the plurality of switches, the PMOS transistor doublet comprises two PMOS transistors, each having a gate, whereby

the gate of the first of the two PMOS transistors is connectable to the first input node via a third switch of the plurality of switches and the gate of the second of the two PMOS transistors is connectable to the second input node via a fourth switch of the plurality of switches.

4. (Currently Amended) The apparatus of claim 3, wherein the gate of the first of the two NMOS transistors is connectable, via a fifth switch of the plurality of switches, to a first reference node being biased with [[a]] the first reference voltage, and the gate of the second of the two NMOS transistors is connectable to the first reference node via a sixth switch of the plurality of switches, and the gate of the first of the two PMOS transistors is connectable, via a seventh switch of the plurality of switches, to a second reference node being biased with [[a]] the second reference voltage and the gate of the second of the two PMOS transistors is connectable to the second reference node via an eighth switch of the plurality of switches.

5. (Previously presented) The apparatus of claim 1, wherein the input stage is a rail-to-rail input stage.

6. (Currently Amended) The apparatus of claim 4, wherein the input stage is configured to keep the NMOS doublet active when the analog input signals are ~~directed~~ coupled to the second differential input and to keep the PMOS transistor doublet active when the analog input signals are coupled ~~directed~~ to the first differential input.

7. (Currently Amended) The apparatus of [[or]] claim 1, wherein said switching signal is a digital switching signal.

8. (Previously presented) The apparatus according to claim 1, wherein transistors serve as the switches.

9. (Previously presented) The apparatus of claim 1 wherein the NMOS transistor doublet and the PMOS transistor doublet are part of a folded cascode rail-to-rail input stage and

wherein the folded cascode rail-to-rail input stage is connected to a second stage comprising a rail-to-rail output stage amplifier.

10. (Currently Amended) An apparatus comprising:

a source driver bank with a plurality of input stages, each input stage having

an NMOS transistor doublet having a first differential input for receiving input signals,

a PMOS transistor doublet having a second differential input for receiving input signals, and

a plurality of switches configured and arranged to, in response to a switching signal, direct analog input signals to one of the first and second differential inputs and to connect the other one of the first and second differential inputs to a reference voltage, the directing of the analog signals causing a ~~to set the~~ ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet to remain constant over the entire input range~~constant~~; and

a bus for receiving input signals.

11. (Previously presented) The apparatus of claim 10, further comprising a gate driver bank and an LCD panel.

12. (Previously presented) The apparatus of claim 10, further comprising a control signal generator for generating the switching signal.

13. (Previously presented) The apparatus of claim 10 being part of a panel module.

14. (Currently Amended) An apparatus comprising

an input stage with an NMOS transistor doublet having a first differential input for receiving input signals, a PMOS transistor doublet having a second differential input for receiving input signals, and a plurality of switches for receiving and selectively directing analog input signals only to one of either said first differential input or said second differential input responsive to a switching signal and for connecting the other

one of the first and second differential inputs to a reference voltage responsive to the switching signal, ~~wherein~~ the input stage being [[is]] configured to keep the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant over the entire input range by operating ~~operate~~ in either a first mode or a second mode responsive to the switching signal, ~~and~~ the NMOS and PMOS transistor doublets each being ~~are both~~ kept active in each of the modes, ~~and wherein~~ the plurality of switches being ~~are~~ configured, in the first mode, to direct the analog input signals to the first differential input and to connect a first reference voltage to the second differential input, and the plurality of switches ~~are~~ being configured, in the second mode, to direct the analog input signals to the second differential input and to connect a second reference voltage to the first differential input~~, and whereby the input stage is configured to keep the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant~~.

15. (Previously presented) The apparatus of claim 1, wherein the first differential input is formed by the gates of the NMOS transistor doublet and the second differential input is formed by the gates of the PMOS transistor doublet.

16. (Previously presented) The apparatus of claim 1, wherein the plurality of switches are configured to selectively direct input signals to one of the differential inputs, and to connect the other one of the differential inputs to a reference voltage, to keep the transconductance ratios of the NMOS and PMOS transistor doublets constant.

17. (Cancelled).

18. (New) The apparatus of claim 1, wherein the input stage is configured to:

couple transistor gates of the NMOS transistor doublet to a high reference voltage when the analog input signals are directed to the second differential input; and

couple transistor gates of the PMOS transistor doublet to a low reference voltage when the analog input signals are directed to the first differential input.

19. (New) The apparatus of claim 1, wherein the input stage is configured to:

cause the NMOS transistor doublet to exhibit a constant transconductance when the analog input signals are directed to the second differential input; and

cause the NMOS transistor doublet to exhibit a constant transconductance when the analog input signals are directed to the first differential input.

20. (New) The apparatus of claim 1, wherein the reference voltage is a constant voltage.

21. (New) The apparatus of claim 1, wherein the apparatus is configured to exhibit a constant offset over the entire input range.